In the Claims:

1. (Currently Amended) A method for fabricating an integrated pin diode ~~(14), in particular a pin photodiode (14), having the following steps executed without a restriction by the order specified~~:

~~production of~~ producing a doped region ~~(20)~~ of one conduction type~~,~~ which~~,~~ ~~in respect of~~is near a carrier substrate~~;~~ ~~(12), is near the substrate,~~

~~production of~~ producing a doped region ~~(42)~~ remote from the substrate, which is further away from the carrier substrate ~~(12)~~ than the region ~~(20)~~ near the substrate and is of a different conduction type than the conduction type of the region ~~(20)~~ near the substrate~~;~~~~,~~

producing ~~production of~~ an intermediate region ~~(30)~~, which is arranged between the region ~~(20)~~ near the substrate and the region ~~(42)~~ remote from the substrate and is undoped or provided with a weak doping in comparison with the doping of the region ~~(20)~~ near the substrate and the doping of the region ~~(42)~~ remote from the substrate~~,~~~~;~~

producing ~~and production of~~ at least one electrically conductive terminal region ~~(32)~~, which leads to the region ~~(20)~~ near the substrate, in a layer ~~(55)~~ containing the intermediate region ~~(30)~~~~;~~

producing a doped decoupling region at the same time as the region near the substrate, the decoupling region having the same conduction type as the region near the substrate;

producing a circuit arrangement carried by the carrier substrate and containing at least two electronic components; and

producing a circuit substrate, which is arranged between the decoupling region and at least one of the components, and the circuit substrate forming a pn diode or an np diode with the decoupling region,

the decoupling region being arranged between one portion of the components and the carrier substrate and not between the other portion of the components and the carrier substrate, and

in the layer containing the intermediate region and in which the region near the carrier substrate and the decoupling region are arranged, regions outside the region near the substrate and the decoupling region are

provided with a doping of a different conduction type from the region near the substrate and the decoupling region or are undoped.

2. (Currently Amended) The method as claimed in claim 1, wherein the terminal region ~~(32)~~ penetrates through the layer ~~(55)~~ from ~~its~~ an interface remote from the substrate as far as ~~its~~ an interface near the substrate.

3. (Cancelled)

4. (Currently Amended) The method as claimed in claim ~~3~~1, comprising the step of producing ~~production of~~ an electrically conductive decoupling region terminal region ~~(56)~~ at the same time as the production of the terminal region ~~(32)~~ leading to the region ~~(20)~~ near the substrate.

5. (Currently Amended) The method as claimed in claim 4, wherein the decoupling region terminal region ~~(56)~~ and the decoupling region ~~(22)~~ form a shielding well which completely surrounds a region encompassed by the shielding well ~~completely or, relative to the side areas and the~~ a base area ~~of the encompassed region, by at least fifty percent or by at least seventy five percent~~.

6. (Currently Amended) The method as claimed in ~~one of~~ claims ~~3~~4 ~~to 5~~, wherein,

in the layer ~~(55)~~ in which the region ~~(20)~~ near the substrate and the decoupling region ~~(22)~~ are arranged, the regions outside ~~said regions (20, 22)~~ the region near the substrate and the decoupling region are provided with a doping of a different conduction type, an oxide ~~(130)~~ covering the region ~~(20)~~ near the substrate and the decoupling region ~~(22) preferably servingserve~~ for masking implantation ~~(140), or~~

~~wherein, in the layer (55) in which the region (20) near the substrate and the decoupling region (22) are arranged, the regions outside said regions (20) are undoped or selectively doped~~.

7. (Currently Amended) The method as claimed in ~~one of the preceding claimsclaim~~ 1, wherein at least one of:

the terminal region ~~(32, 56)~~ is produced with ~~the~~ fabrication of a trench ~~which preferably has a depth that is at least twice its width, or wherein~~;

the terminal region ~~(32, 56)~~ is fabricated with the aid of a diffusion process in which dopants diffuse from a region remote from the substrate as far as the layer ~~(20)~~ near the substrate~~,~~; and

~~and/or wherein~~ the terminal region ~~(32, 56)~~ is produced by an implantation method~~, preferably by a high-energy implantation method~~.

8. (Currently Amended) The method as claimed in ~~one of the preceding claims~~claim 1, wherein at least one of:

the layer ~~(55)~~ containing the intermediate region ~~(30)~~ is produced by an epitaxy method~~,~~; and

~~and/or wherein~~ a base material for an embedding region ~~(52, 54)~~, which serves for embedding components ~~(58, 60, 82)~~ of an integrated circuit arrangement ~~(10)~~, is produced simultaneously during the epitaxy method.

9. (Currently Amended) The method as claimed in claim 8, wherein an epitaxy method for producing an epitaxial layer is conducted in at least two stages,

the epitaxial growth being interrupted,

the interruption being followed by ~~the~~ execution of at least one other process, and ~~preferably a doping process for fabricating a doping which differs from a doping of the epitaxial layer,~~

~~and~~ the growth of the epitaxial layer being continued after the execution of the at least one other process.

10. (Currently Amended) The method as claimed in ~~one of the preceding claims~~claim 1, wherein the terminal region ~~(32)~~ leading to the region ~~(20)~~ near the substrate laterally encompasses the intermediate region ~~(30), preferably completely~~.

11. (Currently Amended) The method as claimed in ~~one of the preceding claims~~claim 1, wherein the layer ~~(55)~~ containing the intermediate

region ~~(30)~~ is a semiconductor layer which ~~preferably~~ contains regions with different conduction types.

12. (Currently Amended) The method as claimed in ~~one of the preceding claims~~claim 1, wherein the decoupling region ~~(22)~~ adjoins material ~~(12, 52, 54)~~ with a different conduction type or is surrounded by material with a different conduction type~~, preferably on all sides apart from one or a plurality of decoupling region terminal regions (56)~~.

13. (Currently Amended) An integrated circuit arrangement ~~(10)~~ having a pin diode ~~(14), in particular having a pin photodiode (14),~~ comprising:

~~having~~ a carrier substrate ~~(12),~~ which carries a region sequence of a pin diode ~~(14),~~;

~~having~~ a doped region ~~(20)~~ of one conduction type, which is contained in the region sequence and is near the substrate;~~,~~

~~having~~ a doped region ~~(42)~~ remote from the substrate, which is contained in the region sequence, is further away from the carrier substrate than the region near the substrate, and is of a different conduction type than the conduction type of the region ~~(20)~~ near the substrate~~,~~;

~~having~~ an intermediate region ~~(30)~~ which is arranged between the region ~~(20)~~ near the substrate and the region ~~(42)~~ remote from the substrate and is undoped or provided with a weak doping in comparison with the doping of the region ~~(20)~~ near the substrate and the doping of the region ~~(42)~~ remote from the substrate~~,~~;

~~and having~~ an electrically conductive terminal region ~~(32)~~, which leads to the region ~~(20)~~ near the substrate and is arranged in a layer ~~(55)~~ containing the intermediate layer ~~(30)~~;

a circuit arrangement carried by the carrier substrate and containing at least two electronic components;

a doped decoupling region arranged between one component and the carrier substrate and of the same conduction type as the region near the substrate and arranged in one plane with the region near the substrate; and

a circuit substrate, which is arranged between the decoupling region and at least one of the components, the circuit substrate forming a pn diode or an np diode with the decoupling region,

the decoupling region being arranged between one portion of the components and the carrier substrate and not between the other portion of the components and the carrier substrate, and

in the layer containing the intermediate layer and in which the region near the substrate and the decoupling region are arranged, regions outside the region near the substrate and the decoupling region are provided with a doping of a different conduction type or are undoped.

14. (Currently Amended) The circuit arrangement ~~(10)~~ as claimed in claim 13, wherein the terminal region ~~(32)~~ penetrates through the layer ~~(55)~~ from ~~its~~ an interface remote from the substrate as far as ~~its~~ an interface near the substrate.

15. (Currently Amended) The circuit arrangement ~~(10)~~ as claimed in claim 13 ~~or 14~~, further ~~comprising a circuit arrangement (10) which is carried by the carrier substrate (12) and contains at least two electronic components carried by the carrier substrate~~ (58, 60, 82), and a doped decoupling region ~~(22) arranged between the one of the components (58) and the carrier substrate, (12) and~~ wherein the decoupling region ~~of the same conduction type as the region (20) near the substrate and/or of~~has the same dopant concentration as the region ~~(20)~~ near the substrate ~~and/or arranged in one plane with the region (20) near the substrate~~.

16. (Currently Amended) The circuit arrangement ~~(10)~~ as claimed in claim 15, further comprising an electrically conductive decoupling region terminal region ~~(56)~~, at least one of:

which leads to the decoupling region; ~~(22)~~ and/~~or~~

which has the same material composition as the terminal region ~~(32)~~ leading to the region ~~(20)~~ near the substrate.

17. (Cancelled)

18. (New) The method as claimed in claim 7, wherein a depth of the trench is at least twice a width of the trench.

19. (New) The method as claimed in claim 9, wherein the at least one other process comprises a doping process for fabricating a doping which differs from a doping of the epitaxial layer.

20. (New) The method as claimed in claim 10, wherein the terminal region leading to the region near the substrate completely laterally encompasses the intermediate region.

21. (New) The method as claimed in claim 12, wherein the decoupling region is surrounded by the material with a different conduction type on all sides apart from one or a plurality of decoupling region terminal regions.

22. (New) The method as claimed in claim 4, wherein the decoupling region terminal region and the decoupling region form a shielding well which surrounds a region encompassed by the shielding well, relative to the side areas and the base area of the encompassed region, by at least fifty percent or by at least seventy five percent.